• .	Application No.	Applicant(s)
Notice of Allowability	09/963,480	AWAKA ET AL.
	Examiner	Art Unit
	Chat C. Do	2193
The MAILING DATE of this communication appears on the cover sheet with the correspondence address All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS. This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.		
1. This communication is responsive to <u>08/02/2007</u> .		
2. The allowed claim(s) is/are <u>1, 3, 10, 12, and 19-20, renumbered as 1-6.</u>		
3.		
Attachment(s) 1. Notice of References Cited (PTO-892) 2. Notice of Draftperson's Patent Drawing Review (PTO-948) 3. Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 4. Examiner's Comment Regarding Requirement for Deposit of Biological Material	5. Notice of Informal F 6. Interview Summary Paper No./Mail Da 7. Examiner's Amenda 8. Examiner's Statema	r (PTO-413), tte

REASONS FOR ALLOWANCE

- 1. Claims 1, 3, 10, 12, and 19-20 are allowed.
- 2. Claims 2, 4-9, 11, and 13-18 are cancelled.
- 3. The following is an examiner's statement of reasons for allowance:

The prior art of records fails to disclose or render an obviousness of a multiplyaccumulate module comprising: a plurality of Booth encoder and decoder cells; a plurality of Wallace tree cells connected to the Booth decoder cells; wherein the module includes a plurality of electrical paths including at least one critical path being an electrical path as an electrical signal to travel from an input of the module core to an output of the module core is greater than or equal to a predetermined amount of time and less than the longest timing path; the plurality of Booth decoder cells including at least first and second Booth decoder cells wherein at least one of a first plurality of transistors of the first Booth decoder cell is constructed to have a width greater than corresponding one of a second plurality of transistors of the second Booth encoder cell; the plurality of Wallace tree cells including at least one first and second Wallace tree cells wherein at least one of a first plurality of transistors of the first Wallace tree cell is constructed to have a width greater than corresponding one of a second plurality of transistors of the second Wallace tree cell; and wherein the at least first Booth decoder cell and first Wallace tree cell are disposed on the critical path along with other features as cited in independent claims 1, 10, and 19-10.

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The closest found prior arts are Hansen et al. (U.S. Publication No. 2003/01110197 A1) and Itoh (U.S. Publication No. 2001/0009012 A1). Hansen et al. in view of Itoh disclose a multiply-accumulate module comprising a plurality of Booth encoder and decoder cells; a plurality of Wallace tree cells; and a critical timing path. However, Hansen et al. in view of Itoh fail to disclose a structure detail of the critical timing path as a path wherein the at least first Booth decoder cell and first Wallace tree cell are disposed on and wherein the plurality of Booth decoder cells including at least first and second Booth decoder cells wherein at least one of a first plurality of transistors of the first Booth decoder cell is constructed to have a width greater than corresponding one of a second plurality of transistors of the second Booth encoder cell; the plurality of Wallace tree cells including at least one first and second Wallace tree cells wherein at least one of a first plurality of transistors of the first Wallace tree cell is constructed to have a width greater than corresponding one of a second plurality of transistors of the second Wallace tree cell as clearly seen above.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (571) 272-3721. The examiner can normally be reached on Tue-Fri 9:00AM to 7:30PM.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Chat C. Do Examiner Art Unit 2193

September 12, 2007